

## ———— Bachelor Thesis ————

# Scaling SIMD beyond AVX-512

## Description

Vectorization is a key technique for code optimization. It exploits Data Level Parallelism (DLP) by grouping instructions into vectors and applying vector instructions instead of scalar ones. In today's general purpose processors, vectorization is supported by Single Instruction, Multiple Data (SIMD) ISA extensions and hardware. Over the years, these hardware extensions were expanded in terms of vector sizes and number of instructions.

It is the goal of this thesis to analyze if moving beyond the state-of-the-art, i.e. AVX-512, is still beneficial. For this purpose, a set of low-level vectorized benchmarks, i.e. written in intrinsics or assembly, should be analyzed via simulation for already existing SIMD ISAs. Furthermore, this simulation should then be enhanced to support wider vector sizes, so it can be determined when the benefit of SIMDization will diminish due to limited DLP in applications and memory bandwidth requirements.

**Keywords:** SIMD, vectorization, performance modelling, SPEC

## Required Skills

- knowledge in computer architecture
- programming skills in C/C++
- experience with low-level programming, such as intrinsics or assembly

## Desired Skills

- knowledge of performance simulation and modelling

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