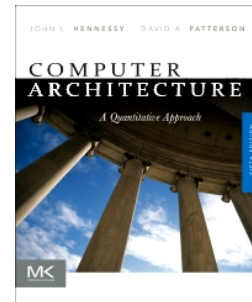


## Bachelor/Master Project

### Limits of Instruction-Level Parallelism 2017

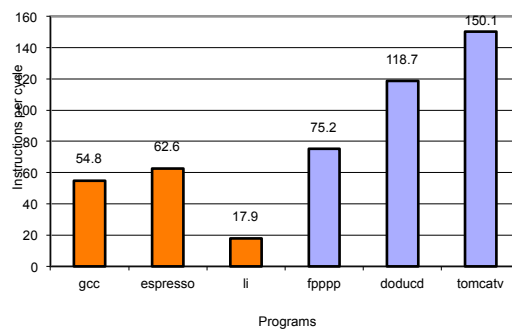
#### Background and Motivation

Modern high-performance processors exploit parallelism between instructions (instruction-level parallelism, ILP) to increase performance. The famous textbook “Computer Architecture – A Quantitative Approach” by John Hennessy and David Patterson [1] contains a section in which the limits of ILP are discussed. This section is based on a study by David Wall in 1993 [2]. The problem with this section is that it is very outdated. Since 1993, substantially better branch predictors, better compilers, etc. have been developed, and the study has been conducted using an ancient benchmark suite (SPEC92).



#### Project Goal

The goal of this project is to repeat and extend Wall’s experiments. To analyze the limits of ILP assuming infinite hardware resources and perfect branch prediction etc., most likely a trace-driven simulator needs to be developed. To measure ILP using realizable hardware, modern processor simulators need to be compared and the best one selected, which then probably needs to be extended. Perhaps we can even convince Hennessy and Patterson to include our results in future editions of the textbook. Depending on the amount of work, this project can be performed as a bachelor or master project.



#### Prerequisites

- Basic computer architecture / organization course.
- The course “Advanced Computer Architecture” offered by AES or a similar course, or the willingness to study Chapter 3 of [1].
- Proficiency in C/C++.

#### Contact

- Ben Juurlink ([b.juurlink@tu-berlin.de](mailto:b.juurlink@tu-berlin.de)).

#### References

- [1] David Patterson and John Hennessy, *Computer Architecture – A Quantitative Approach*, 5<sup>th</sup> edition, Morgan Kaufmann, Paperback ISBN: 9780123838728.
- [2] D. W. Wall, “Limits of instruction-level parallelism,” Digital Western Research Laboratory, Tech. Rep. 93/6, Nov. 1993.